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(54) Title: BURIED CHANNEL STRAINED SILICON FET USING AN ION IMPLANTED DOPED LAYER

(57) Abstract: A buried channel FET including a substrate, a relaxed SiGe layer, a channel layer, a SiGe cap layer, and an ion implanted dopant supply. The ion implanted dopant supply can be in either the SiGe cap layer or the relaxed SiGe layer. In another embodiment, there is provided a circuit including at least one strained channel, enhancement mode FET, and at least one strained channel, depletion mode FET. The depletion mode FET includes an ion implanted dopant supply. In further embodiments, there is provided a method of fabricating a buried channel FET including providing a relaxed SiGe layer on a substrate, providing a channel layer on the relaxed SiGe layer, providing a SiGe cap layer on the channel layer, and ion implanting dopant supply. The dopant supply can be ion implanted in either the SiGe cap layer or the SiGe layer. In yet another embodiment, there is provided a method of fabricating a circuit including providing at least one strained channel, enhancement mode FET, and at least one strained channel, depletion mode FET on a substrate, and ion implanting a dopant supply in the depletion mode FET.

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BURIED CHANNEL STRAINED SILICON FET USING AN ION IMPLANTED DOPED LAYER

PRIORITY INFORMATION

This application claims priority from provisional application Ser. No. 60/207,382 filed May 26, 2000.

BACKGROUND OF THE INVENTION

The invention relates to the field of buried channel strained-Si FETs, and in particular to these FETs using a supply layer created through ion implantation.

The advent of relaxed SiGe alloys on Si substrates introduces a platform for the construction of new Si-based devices. These devices have the potential for wide application due to the low cost of using a Si-based technology, as well as the increased carrier mobility in strained layers deposited on the relaxed SiGe.

As with most new technologies, implementing these advances in a Si CMOS fabrication facility requires additional innovation. For example, some of the potential new devices are more easily integrated into current Si processes than other devices. Since process technology is directly relevant to architecture, particular innovations in process technology can allow the economic fabrication of new applications/architectures.

FIGs. 1A and 1B are schematic block diagrams showing the variety of strained Si devices that are possible to fabricate given the advent of relaxed SiGe buffer layers. FIG. 1A shows a surface channel strained Si MOSFET 100. In this configuration, a tensile, strained Si channel 102 is deposited on relaxed SiGe layer 104 with a Ge concentration in the range of 10-50%. This relaxed SiGe layer is formed on a Si substrate 108 through the use of a compositionally graded SiGe buffer layer 106. A conventional MOS gate stack 110 is on the strained silicon channel and consists of an oxide layer 112, a poly-Si electrode 114, and a metal contact layer 116. Doped source 118 and drain 120 regions are also formed on either side of the gate stack to produce the MOSFET device structure.

A buried channel strained Si high electron mobility transistor (HEMT) 130 is shown in FIG. 1B. In this configuration, the strained Si 102 atop the relaxed SiGe 104 has been capped with a thin SiGe cap layer 132. The strained Si layer generally has a thickness between 2-30nm, while the SiGe cap layer has a thickness between 2-

20nm. A metal Schottky gate 134 on the SiGe cap layer is commonly used on the HEMT, and, as in the MOSFET structure, doped source 118 and drain 120 regions are formed on each side of this gate.

FIG. 1C shows a buried channel strained Si MOSFET 140. This device has the same Si/SiGe layer structure as the HEMT configuration, but with a full MOS gate stack 142, consisting of oxide 144, poly-Si 146, and metal 148 layers, rather than the metal Schottky gate.

It is important to separate these devices into two categories, surface channel devices, of which an embodiment is shown in FIG. 1A, and buried channel devices, of which embodiments are shown in FIGs. 1B and 1C. In the case of the surface channel device, a light background doping in the SiGe during epitaxial growth or by implantation is sufficient to position the Fermi level such that a MOSFET constructed from the strained surface channel has reasonably large threshold values. Thus, the surface can be inverted for either p or n channel operation.

FIGs. 2A and 2B are the energy band diagram for the case of the surface channel FET for an NMOS device, (A) at zero bias, and (B) at a bias to turn on the transistor, respectively. When the transistor is turned on, a relatively large electric field exists in the normal direction to the surface plane, and the electrons are attracted to the surface and operate in the strained Si surface channel. The speed of the transistor is increased due to the fact that the electrons reside in the high mobility, strained Si surface channel. However, the device has noise performance similar to a conventional Si MOSFET since the carriers scatter off the SiO_2/Si interface, and the device, although it possesses a mobility larger than that of a conventional Si device, still has a mobility that is limited by the SiO_2/Si interface.

However, it is known from III-V materials that a buried channel device should possess a much higher electron mobility and lower noise performance. For example, the structures shown in FIG. 1B and C should have higher channel mobility and lower noise performance than the device in FIG. 1A since the electron scatters off a semiconductor interface instead of an oxide interface.

A crucial flaw in the device shown in FIG. 1C that leads to processing difficulties and limitations in circuit layout and architectures is that when the device is biased to invert the channel and turn the device on, the band structure is such that many of the carriers leave the buried channel. FIG. 3 is an energy band diagram showing schematically the problem with a buried channel device in which there is no

dopant supply layer. The field required to turn on the device empties the buried channel. This effectively creates a surface channel device even though the buried channel layer is present in the heterostructure.

The applied gate bias of FIG. 3 has bent the bands such that many of the electrons from the well escape confinement and create an inversion layer at the oxide/semiconductor interface. Since transconductance of a field effect device is high if the mobility and the number of carriers is high, a high performance FET, i.e., even higher performance than the surface channel device, is difficult to achieve. At low vertical fields, the electrons are in the high mobility buried channel, but there are few in number. If the device is turned on and inverted as shown in FIG. 3, the carrier density in the surface channel is high but the mobility is reduced since the carriers are now at the rough oxide interface.

One way to solve this problem is to insert a dopant supply layer into the structure, as shown in FIG. 4A. FIG. 4A is a schematic block diagram of a structure 400 in which the buried channel can be occupied with a high density of electrons via the insertion of a layer of donor atoms. It will be appreciated that an equivalent schematic can be constructed for a buried hole channel with a layer of acceptor atoms.

The structure 400 includes a strained Si channel 402 positioned between two SiGe layers, a relaxed SiGe layer 404 and a thin SiGe cap layer 406. Although FIG. 4A shows a dopant supply layer 408 in the SiGe cap, the dopants can be introduced into either SiGe layer. As has been shown in the III-V buried channel devices, this layer configuration creates a band structure where now the buried channel is occupied, as shown in FIG. 4B. In this figure, the supply layer leads to localized band bending and carrier population of the buried strained Si. In the strained Si, the conduction band has been lowered beneath the Fermi level, resulting in a high carrier density in the high mobility channel. One disadvantage of this structure is that now the transistor is on without any applied voltage, and a voltage is supplied to the gate to turn off the transistor. Thus, this transistor is normally on or depletion-mode. As a result, the device is useful in analog and logic applications, but is not easily implemented in a conventional CMOS architecture.

Common accepted practice in the buried channel heterostructure FETs is to use a dopant supply layer that is introduced in an epitaxial step, i.e., deposited during the epitaxial process that creates the Si/SiGe device structure. This dominant process

originates from the III-V research device community (AlGaAs/GaAs materials system). However, this epitaxial dopant supply layer is undesirable since it reduces thermal budget and limits the variety of devices available in the circuit. For example, if the dopant supply layer is introduced in the epitaxial step, when processing begins, the thermal budget is already constrained due to diffusion of the supply layer dopants. All devices in the circuit must also now be buried channel devices with similar thresholds, since any removal of the dopant layer in a particular region would require complete etching of the local area and removal of critical device regions.

SUMMARY OF THE INVENTION

In accordance with the invention, there is provided a device structure that allows not only the creation of a low-noise, high frequency device, but also a structure that can be fabricated using conventional processes such as ion implantation. The use of ion implantation to create a carrier supply layer also allows great flexibility in creating different types of strained Si devices within the same circuit.

Accordingly, the invention provides a buried channel FET including a substrate, a relaxed SiGe layer, a channel layer, a SiGe cap layer, and an ion implanted dopant supply. The ion implanted dopant supply can be in either the SiGe cap layer or the relaxed SiGe layer. In one embodiment the FET is a MOSFET. In another embodiment the FET is within an integrated circuit. In yet another embodiment, the FET is interconnected to a surface channel FET.

The invention also provides a circuit including at least one strained channel, enhancement mode FET, and at least one strained channel, depletion mode FET. The depletion mode FET includes an ion implanted dopant supply. In exemplary embodiments, the FETs are surface channel or buried channel MOSFETS. In another exemplary embodiment, the FETs are interconnected to form an inverter.

The invention further provides a method of fabricating a buried channel FET including providing a relaxed SiGe layer on a substrate, providing a channel layer on the relaxed SiGe layer, providing a SiGe cap layer on the channel layer, and ion implanting dopant supply. The dopant supply can be ion implanted in either the SiGe cap layer or the relaxed SiGe layer. In another embodiment, there is provided a method of fabricating a circuit including providing at least one strained channel, enhancement mode FET, and at least one strained channel, depletion mode FET on a substrate, and ion implanting a dopant supply in the depletion mode FET.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1A-1C are schematic block diagrams showing a variety of strained Si devices fabricated with relaxed SiGe buffer layers;

FIGs. 2A and 2B are the energy band diagram for the case of the surface channel FET for an NMOS device, at zero bias, and at a bias to turn on the transistor, respectively;

FIG. 3 is an energy band diagram showing schematically the problem with a buried channel device in which there is no dopant supply layer;

FIG. 4A is a schematic block diagram of a structure in which the buried channel can be occupied with a high density of electrons via the insertion of a layer of donor atoms;

FIG. 4B is the energy band diagram for the structure of FIG. 4A;

FIGs. 5A-5I show a process flow in which ion implantation is used to create a buried channel device with an ion implanted dopant supply layer;

FIG. 6 is a schematic block diagram of a structure in which both a surface channel device and buried channel device are configured next to each other on a processed Si/SiGe heterostructure on a Si substrate;

FIG. 7 is a schematic diagram of an inverter utilizing enhancement mode and depletion mode devices as shown in FIG. 6;

FIG. 8A is a schematic block diagram of a structure utilizing the implanted dopant supply layer on buried oxide technology;

FIG. 8B is a schematic block diagram of a structure utilizing the implanted dopant supply layer without the use of a buried SiO_2 layer; and

FIG. 9 is a schematic block diagram of a buried Ge channel MOSFET.

DETAILED DESCRIPTION OF THE INVENTION

Fortunately, there is a solution to the problems described heretofore if one resists following the traditional path for dopant introduction in III-V buried channel devices. In the III-V materials, the dopant supply layer is introduced in the epitaxial step since there is no other known method.

In Si, it is well known that ion implantation can be used to create source/drain regions, and that annealing cycles can be used to remove the damage of such an

implantation. FIGs. 5A-5I show a process flow in which ion implantation is used to create a buried channel device with an ion implanted dopant supply layer. The implanted layer can be an n-type dopant, such as phosphorus (P), arsenic (As), or antimony (Sb), or a p-type dopant, such as boron (B), gallium (Ga), or indium (In). The main features of the process depicted in FIG. 5 are described below. Note that this process flow is only an example of how the dopant supply layer can be used in combination with a conventional Si process flow to yield new devices and device combinations. This particular process flow was chosen since it is simple, and produces a depletion-mode buried strained channel device that has use in analog applications.

The process flow in FIG. 5A starts with a field oxidation process. Although this type of isolation can be convenient for larger gate sizes, it should be realized that at shorter gate lengths, trench isolation is preferable. FIG. 5A shows the starting substrate 500 after deposition of the SiO_2 502 and a SiN_x hardmask 504, and definition of the active area 508 and field areas 510 with a photoresist 506 and etch. In order to prevent biasing from creating of conduction paths below the field oxide, a channel-stop implant 512 is performed before the field oxidation using the photoresist, SiO_2 and SiN_x as a mask, as shown in FIG. 5B.

Subsequently, the photoresist is removed and a field oxide 514 is grown. FIG. 5C shows the device structure after completion of the field oxidation step. The field area has been oxidized, and the SiO_2/SiN_x hardmask is still present above the device active area. After stripping the field oxide hardmask materials and creating a sacrificial oxide 516, as shown in FIG. 5D, the sacrificial oxide is stripped and gate oxidation is performed. In the heterostructures described, the strained Si channel in the surface channel MOSFET can be oxidized directly. For buried channel structures, a thin sacrificial Si layer must be present on the surface for oxidation since oxidizing SiGe directly tends to create a high interface state density. Polysilicon 520 deposition atop the gate oxide 518 completes the deposition of the gate stack of the MOSFET. For reduced gate resistance, a titanium silicide 522 can be formed before the gate etch, to reduce the resistance to the gate for RF and other high-speed applications. FIG. 5E depicts the formation of this silicided gate stack after deposition of polysilicon, deposition of titanium, and reaction of the titanium to form the silicide.

The key dopant supply layer implant can be done before or after the gate

oxidation step. A shallow implant is performed in order to place the dopants near the strained Si channel layer. In the exemplary sequence, the dopant supply layer is implanted through the sacrificial oxide indicated in FIG. 5D. In that way, the sacrificial oxide can be stripped after implant, allowing a re-oxidation for achieving the highest gate oxide quality. FIGs. 5F-5I show the remainder of the process, which is standard Si CMOS processing. FIG. 5F shows the device structure after ion implantation of source-drain extensions 524. Next, SiO_2/SiN_x spacers 526 are formed by deposition and an anisotropic etch, resulting in the structure pictured in FIG. 5G. Afterward, the deep source-drain ion implants 528 are performed, and the source-drain regions are silicided, as shown in FIG. 5H. The source-drain silicide 530 is typically formed via metal deposition, annealing, and removal of unreacted metal. Finally the interlayer dielectric, in this case SiO_2 532 is deposited over the entire device structure. Contact cuts to the source, drain, and gate are etched away, and the first metallization layer 534 is deposited. FIG. 5I shows the device after the completion of all of the process steps.

It will be appreciated that one objective of the invention, and the process in general, is to inject the advantages of strained-Si technology into the current Si manufacturing infrastructure. The further one deviates from these typical Si processes, the less impact the strained-Si will have. Thus, by utilizing the implanted dopant supply layer described herein, the device design capability is increased, and manufacturability is improved. If the dopant supply layer were created by the conventional method of doping during epitaxial growth, the flexibility would be less, leading to non-typical architectures, different manufacturing processes, and procedures that differ much more significantly from typical process flows. The flow described in FIGs. 5A-5I is compatible with current Si VLSI processing and thus is more likely to have widespread impact.

As one can see with the above process, the goals of creating a new Si-based device are achieved by producing a highly populated buried channel, yet the dopants were not inserted at the very beginning of the process through epitaxy. Although ion implantation may not produce a dopant profile that is as abrupt as a profile created through epitaxy, and thus the electron mobility in the buried channel may decrease slightly, the manufacturability of this process is far superior. In addition, the combination of buried channel devices and surface channel devices on the same wafer is enabled, since the local presence or absence of the implantation process will create

a buried channel or surface channel device, respectively. Furthermore, buried channel devices can be created on the same wafer and within the same circuit with different thresholds by choosing the implant dose and type.

An example is shown in FIG. 6 that shows a structure 600 in which both a surface channel device 650 and buried channel device 660 are configured next to each other on a processed Si/SiGe heterostructure on a Si substrate 608. The elements of the buried channel device are the same as shown in FIG. 1C while the elements of the surface channel device are the same as shown in FIG. 1A. The depletion mode, buried channel device results from the incorporation of a dopant supply implant 670. Other devices on the wafer, like the enhancement mode device 650, can be masked off and not receive the supply implant. The SiGe cap layer can be removed 632, if desired, forming surface channel enhancement mode strained Si devices in these regions. In the case where the dopant supply layer is grown epitaxially and embedded in the wafer from the beginning, integration of conventional MOS devices with the buried channel device is difficult, since the MOS devices must not contain the dopant supply layer.

The ability to mix these devices on a common chip area is a great advantage when creating system-on-chip applications. For example, the low noise performance and high frequency performance of the buried channel devices suggest that ideal applications are first circuit stages that receive the electromagnetic wave in a wireless system. The ability to form such devices and integrate them with surface channel MOS devices shows an evolutionary path to system-on-chip designs in which the entire system from electromagnetic wave reception to digital processing is captured on a single Si-based chip.

In such a system, there is a trade-off in circuit design in passing from the very front-end that receives the electromagnetic signal to the digital-end that processes the information. In general, the front-end requires a lower level of complexity (lower transistor count), but a higher performance per transistor. Just behind this front-end, it may be advantageous (depending on the application) to design higher performance digital circuits to further translate the signal received by the front end. Finally, when the signal has been moved down to lower frequencies, high complexity MOS circuits can be used to process the information. Thus, the buried channel MOSFET has an excellent application in the very front-end of analog/digital systems. The buried channel MOSFET will offer low noise performance and a higher frequency of

operation than conventional Si devices.

For just behind the front-end, in some applications it may be desirable to have high-performance logic. In FIG. 6 the surface channel device 650 is an enhancement-mode device (turned off without applied gate bias) and the buried channel device 660 can be a depletion-mode device (turned on without applied gate voltage) or an enhancement mode device, depending on the implant conditions. Thus, the device combination shown in FIG. 6 can be used to create enhancement-depletion logic, or E/D logic. An example of an inverter 700 using this combination of devices is shown in FIG. 7. The E/D inverter 700 is virtually identical to a typical CMOS inverter, but utilizes enhancement mode 702 and depletion mode 704 devices rather than NMOS and PMOS devices. This fundamental unit of digital design shows that the process described herein is critical in creating high performance circuits for analog applications such as wireless applications and high-speed electronic circuitry.

The enhanced performance is directly related to the mobility of the carriers in the strained Si and the low noise figure of the buried channel device. The enhanced mobility will increase the transconductance of the field effect transistor. Since transconductance in the FET is directly related to power-delay product, logic created with this E/D coupling of the strained devices described herein can have a fundamentally different power-delay product than conventional Si CMOS logic. Although the architecture itself may not be as low power as conventional CMOS, the lower power-delay product due to strained Si and/or buried channels can be used either to increase performance through higher frequency operation, or to operate at lower frequencies while consuming less power than competing GaAs-based technologies. Moreover, since the devices are based on a Si platform, it is expected that complex system-on-chip designs can be accommodated at low cost.

To achieve an even lower power-delay product in the devices, it is possible to employ this process on strained-Si/relaxed SiGe on alternative substrates, such as SiO_2/Si or insulating substrates. FIG. 8A is a schematic block diagram of a structure 800 utilizing the implanted dopant supply layer on buried oxide technology. FIG. 8A shows the same types of devices and elements depicted in FIG. 6 processed on a slightly different substrate. This substrate, a hybrid of relaxed SiGe and SOI substrates, incorporates a buried SiO_2 layer 880 beneath a thin layer of relaxed SiGe 804. Just as with the relaxed SiGe platform illustrated FIG. 6, strained Si devices can be formed atop this new substrate. The buried oxide layer provides the advantages of

a SOI-like substrate, including lower power consumption and decreased junction leakage.

If the substrate shown in FIG. 8A does not have a buried SiO_2 layer, then the structure 890 shown in FIG. 8B is produced. This embodiment is useful in high power applications where the low thermal conduction of a SiGe graded buffer (FIG. 6) or an oxide layer (FIG. 8A) leads to the accumulation of heat in the resulting circuit.

Since the mobility in the buried channel can be in the range of 1000-2900 cm^2/V-sec, and the mobility of the surface channel can be as high as 400-600 cm^2/V-sec, the power-delay product in a conventional Si E/D design will be much larger than the power-delay product for the strained-Si E/D design. Thus, analog chips containing high performance strained Si devices using the ion implant methodology will have a significantly lower power-delay product, which means the chips can have higher performance in a wide-range of applications.

The exemplary embodiments described have focused on the use of ion implantation in strained Si devices; however, the benefits of ion implantation can also be realized in surface and buried channel strained Ge devices. FIG. 9 is a schematic block diagram of a buried Ge channel MOSFET 900. In this embodiment, a relaxed SiGe layer 904 has a Ge concentration in the range of 50-90% Ge. The higher Ge concentration in the relaxed SiGe layer is necessary to ensure that the thickness of the Ge channel 902, which is compressively strained, is not limited by critical thickness constraints. In FIG. 9, the relaxed SiGe layer is shown on a SiGe graded buffer layer 904 on a Si substrate 908. However, the layer can be directly on a Si substrate or a Si substrate coated with SiO_2. Like the Si buried channel device, the MOSFET contains a SiGe cap layer 932, usually with a similar Ge concentration as the relaxed SiGe layer, a gate stack 942 containing oxide 944, poly-Si 946 and metal 948 layers, and doped source 918 and drain 920 drain regions at each end of the gate. The ion implanted dopant supply layer can be introduced into either the SiGe cap layer or the relaxed SiGe layer.

In summary, the ion-implantation methodology of forming the dopant supply layer allows the creation of a manufacturable buried channel MOSFET or MODFET. The methodology also has the advantage that process flows can be created in which depletion-mode transistors can be fabricated by local implantation, but other nearby devices can be shielded from the implant or implanted with different doses/impurities,

leading to enhancement-mode devices. Co-located enhancement and depletion mode devices can further be utilized to create simple digital building blocks such as E/D-based logic. Thus, the invention also leads to additional novel high-performance Si-based circuits that can be fabricated in a Si manufacturing environment.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A buried channel FET comprising:
a substrate;
a relaxed SiGe layer;
a channel layer;
a SiGe cap layer; and
an ion implanted dopant supply.

2. The FET of claim 1, wherein the substrate comprises Si.

3. The FET of claim 1, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

4. The FET of claim 1, wherein the substrate comprises Si with a layer of SiO_2.

5. The FET of claim 1 further comprising a metal-oxide-semiconductor gate.

6. The FET of claim 1, wherein the ion implanted dopant supply is in the SiGe cap layer.

7. The FET of claim 1, wherein the ion implanted dopant supply is in the relaxed SiGe layer.

8. The FET of claim 1, wherein the channel layer is under tensile strain.

9. The FET of claim 1, wherein the channel layer is under compressive strain.

10. The FET of claim 1, wherein the ion implanted dopant supply comprises As, P, Sb, B, Ga, or In.

11. The FET of claim 8, wherein the relaxed SiGe layer has a Ge concentration in the range of 10-50%.

12. The FET of claim 11, wherein the channel layer comprises Si.

13. The FET of claim 12, wherein the ion implanted dopant supply comprises P, As, or Sb.

14. The FET of claim 9, wherein the relaxed SiGe layer has a Ge concentration in the range of 50-90%.

15. The FET of claim 14, wherein the channel layer comprises Ge.

16. The FET of claim 15, wherein the ion implanted dopant supply comprises B, Ga, or In.

17. The FET of claim 1, wherein the channel layer has a thickness between 2 and 30nm.

18. The FET of claim 1, wherein the SiGe cap layer has a thickness between 2 and 20nm.

19. In an integrated circuit, the FET of claim 1.

20. In an integrated circuit, the FET of claim 1 interconnected to a surface channel FET.

21. A buried channel MOSFET comprising:
a substrate;
a relaxed SiGe layer;
a channel layer;
a SiGe cap layer; and
an ion implanted dopant supply in said SiGe cap layer.

22. The MOSFET of claim 21, wherein the substrate comprises Si.

23. The MOSFET of claim 21, wherein the substrate comprises relaxed graded composition SiGe layers on Si.

24. The MOSFET of claim 21, wherein the substrate comprises Si with a layer of SiO_2.

25. The MOSFET of claim 21, wherein the relaxed SiGe layer has a Ge composition in the range of 10-50%.

26. The MOSFET of claim 25, wherein the channel layer comprises Si.

27. The MOSFET of claim 26, wherein the ion implanted dopant supply comprises P, As, or Sb.

28. In an integrated circuit, the MOSFET of claim 21.

29. In an integrated circuit, the MOSFET of claim 21 interconnected to a surface channel MOSFET.

30. A circuit comprising:
at least one strained channel, enhancement mode FET; and
at least one strained channel, depletion mode FET, wherein
said depletion mode FET comprises an ion implanted dopant supply.

31. The circuit of claim 30, wherein the enhancement mode FET is a MOSFET.

32. The circuit of claim 30, wherein the depletion mode FET is a MOSFET.

33. The circuit of claim 30, wherein the enhancement mode FET is a surface channel MOSFET.

34. The circuit of claim 33, wherein the depletion mode FET is a buried channel MOSFET.

35. The circuit of claim 30, wherein the depletion mode FET is a surface channel MOSFET.

36. The circuit of claim 30, wherein the enhancement mode FET is a buried channel MOSFET.

37. The circuit of claim 30, wherein the depletion mode FET is a buried channel MOSFET.

38. The circuit of claim 30, wherein the circuit is an inverter.

39. The circuit of claim 30, wherein the enhancement mode FET and the

depletion mode FET are interconnected to form an inverter.

40. An inverter comprising:
a strained buried channel depletion mode FET; and
a strained surface channel enhancement mode FET, wherein
said strained buried channel depletion mode FET comprises an ion implanted dopant supply.

41. In an integrated circuit, the inverter of claim 40.

42. An inverter comprising:
a strained buried channel depletion mode MOSFET; and
a strained surface channel enhancement mode MOSFET, wherein
said strained buried channel depletion mode MOSFET comprises an ion implanted dopant supply.

43. In an integrated circuit, the inverter of claim 42.

44. A method of fabricating a buried channel FET comprising:
providing a relaxed SiGe layer on a substrate;
providing a channel layer on said relaxed SiGe layer;
providing a SiGe cap layer on said channel layer; and
ion implanting a dopant supply.

45. A method of fabricating a buried channel MOSFET comprising:
providing a relaxed SiGe layer on a substrate;
providing a channel layer on said relaxed SiGe layer;
providing a SiGe cap layer on said channel layer; and
ion implanting a dopant supply in said SiGe cap layer.

46. A method of fabricating a circuit comprising:
providing at least one strained channel, enhancement mode FET and at least one strained channel, depletion mode FET on a substrate; and
ion implanting a dopant supply in said depletion mode FET.

47. A method of fabricating an inverter comprising:
providing a strained buried channel depletion mode FET and a strained surface

channel enhancement mode FET on a substrate; and

ion implanting a dopant supply in said strained buried channel depletion mode FET.

48. A method of fabricating an inverter comprising:

providing a strained buried channel depletion mode MOSFET and a strained surface channel enhancement mode MOSFET on a substrate; and

ion implanting a dopant supply in said strained buried channel depletion mode MOSFET.

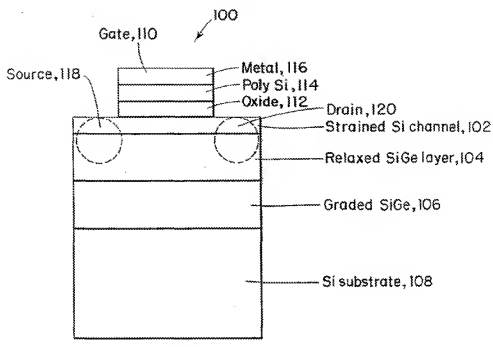
100
Gate, 110
Source, 118
Metal, 116
Poly Si, 114
Oxide, 112
Drain, 120
Strained Si channel, 102
Relaxed SiGe layer, 104
Graded SiGe, 106
Si substrate, 108

FIG. 1A

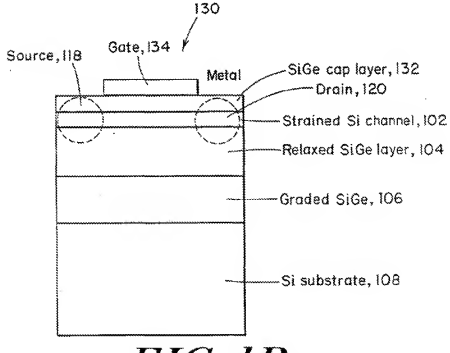
130
Source, 118
Gate, 134
Metal
SiGe cap layer, 132
Drain, 120
Strained Si channel, 102
Relaxed SiGe layer, 104
Graded SiGe, 106
Si substrate, 108

FIG. 1B

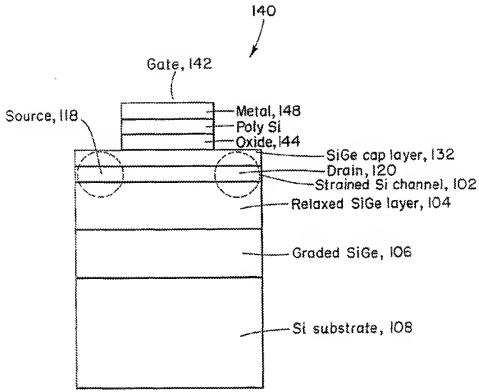
140
Gate, 142
Source, 118
Metal, 148
Poly Si
Oxide, 144
SiGe cap layer, 132
Drain, 120
Strained Si channel, 102
Relaxed SiGe layer, 104
Graded SiGe, 106
Si substrate, 108

FIG. 1C

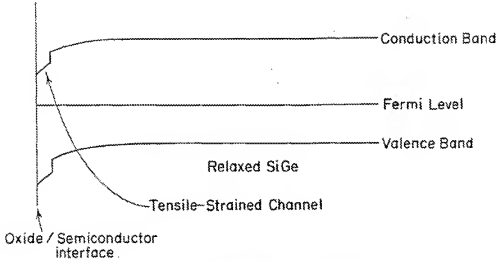
Conduction Band
Fermi Level
Valence Band
Relaxed SiGe
Tensile-Strained Channel
Oxide / Semiconductor interface

FIG. 2A

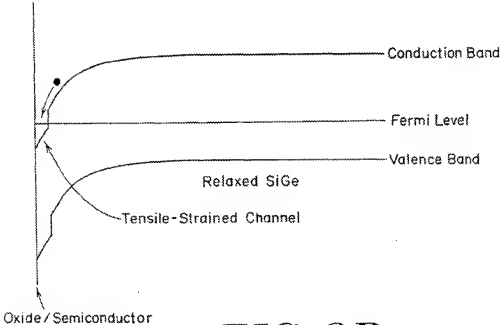
Conduction Band
Fermi Level
Valence Band
Relaxed SiGe
Tensile-Strained Channel
Oxide / Semiconductor

FIG. 2B

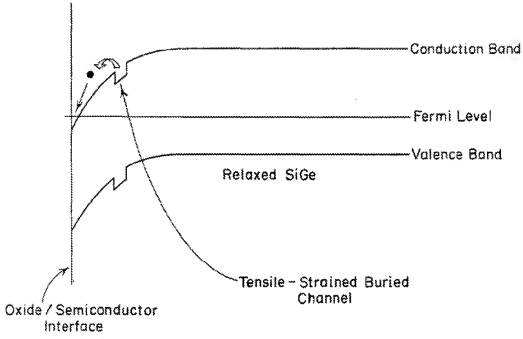
Conduction Band
Fermi Level
Valence Band
Relaxed SiGe
Tensile – Strained Buried Channel
Oxide / Semiconductor Interface

FIG. 3

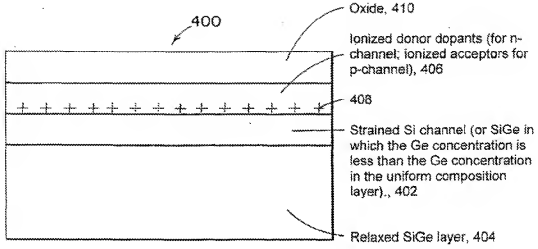
400
Oxide, 410
Ionized donor dopants (for n-channel; ionized acceptors for p-channel), 406
408
Strained Si channel (or SiGe in which the Ge concentration is less than the Ge concentration in the uniform composition layer)., 402
Relaxed SiGe layer, 404

FIG. 4A

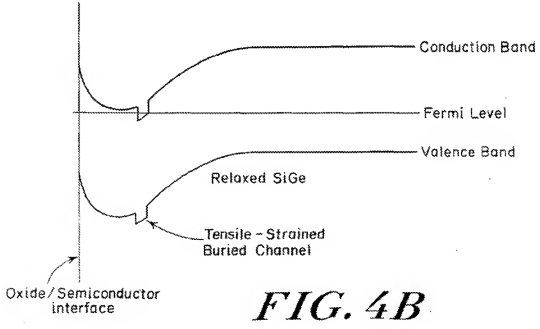
Conduction Band
Fermi Level
Valence Band
Relaxed SiGe
Tensile - Strained Buried Channel
Oxide/Semiconductor interface

FIG. 4B

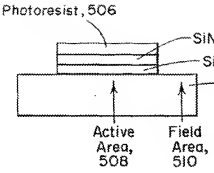

FIG. 5A

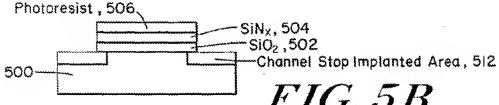

FIG. 5B

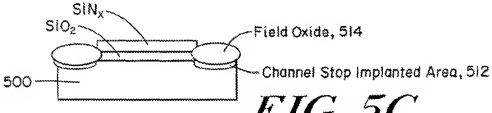

FIG. 5C

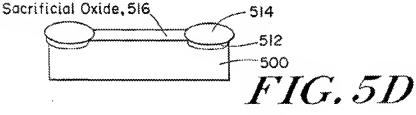

FIG. 5D

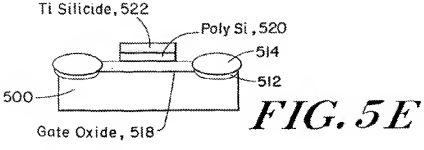

FIG. 5E

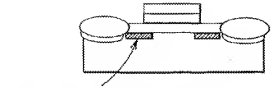

FIG. 5F

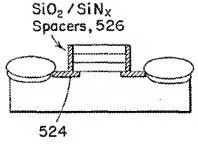

FIG. 5G

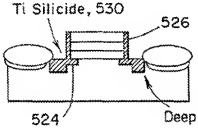

FIG. 5H

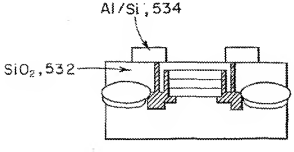

FIG. 5I

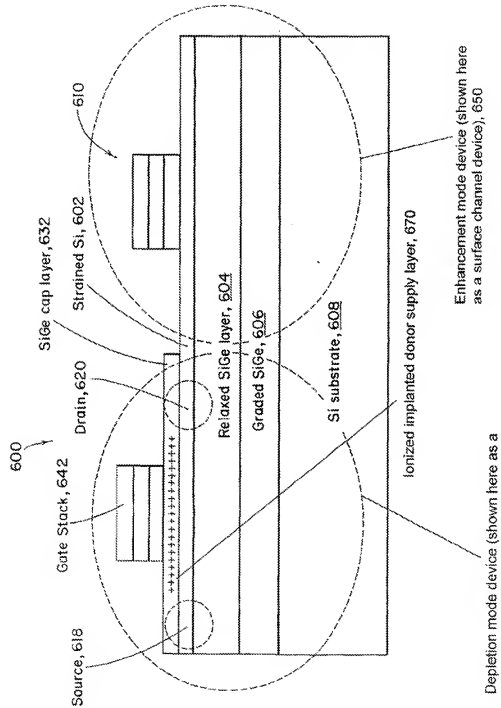
600
Source, 618
Gate Stack, 642
Drain, 620
SiGe cap layer, 632
Strained Si, 602
610
Relaxed SiGe layer, 604
Graded SiGe, 606
Si substrate, 608
Ionized implanted donor supply layer, 670
Depletion mode device (shown here as a buried channel device) created through implantation of dopant supply layer, 660
Enhancement mode device (shown here as a surface channel device), 650

FIG. 6

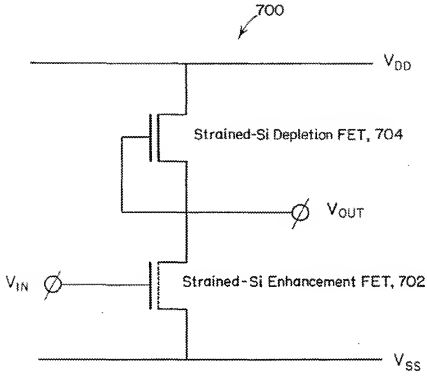
700
V_{DD}
Strained-Si Depletion FET, 704
V_{OUT}
V_{IN}
Strained-Si Enhancement FET, 702
V_{SS}

FIG. 7

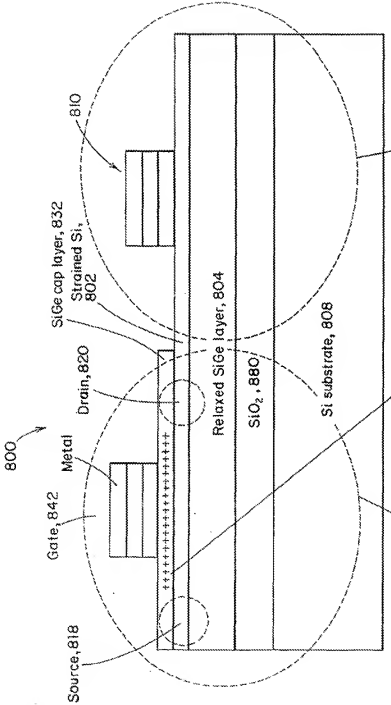
800
Source, 818
Gate, 842
Metal
Drain, 820
SiGe cap layer, 832
Strained Si, 802
Relaxed SiGe layer, 804
SiO_2, 880
Si substrate, 808
Ionized implanted donor supply layer, 870
810
Enhancement mode device (shown here as a surface channel device), 850
Depletion mode device (shown here as a buried channel device) created through implantation of dopant supply layer, 860

FIG. 8A

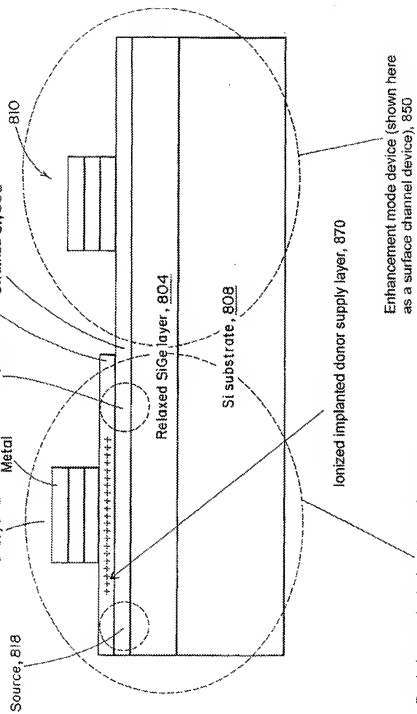
890
Source, 818
Gate, 842
Metal
Drain, 820
SiGe cap layer, 832
Strained Si, 802
810
Relaxed SiGe layer, 804
Si substrate, 808
Ionized implanted donor supply layer, 870
Enhancement mode device (shown here as a surface channel device), 850
Depletion mode device (shown here as a buried channel device) created through implantation of dopant supply layer, 860

FIG. 8B

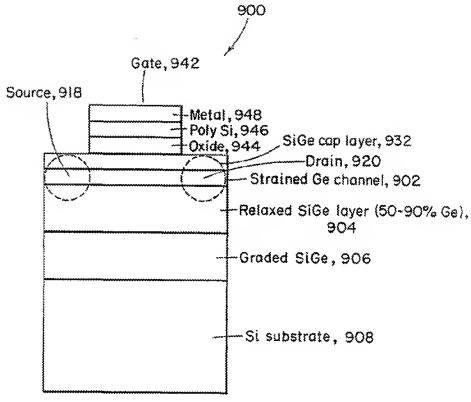
900
Gate, 942
Source, 918
Metal, 948
Poly Si, 946
Oxide, 944
SiGe cap layer, 932
Drain, 920
Strained Ge channel, 902
Relaxed SiGe layer (50-90% Ge), 904
Graded SiGe, 906
Si substrate, 908

FIG. 9

INTERNATIONAL SEARCH REPORT

Int ernat Application No
PCT/US 01/15892

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/778 H01L29/78 H01L29/10 H01L21/20 H01L27/088
H01L21/335 H01L29/786

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 906 951 A (CHU JACK OON ET AL) 25 May 1999 (1999-05-25)	1,2,4-8, 10-14, 19,21, 22, 24-28, 44,45
Y	the whole document	3,15,16, 23,30-43
Y	MAITI K ET AL: "STRAINED-SI HETEROSTRUCTURE FIELD EFFECT TRANSISTORS" SEMICONDUCTOR SCIENCE AND TECHNOLOGY, INSTITUTE OF PHYSICS. LONDON, GB, vol. 13, no. 11, 1 November 1998 (1998-11-01), pages 1225-1246, XP000783138 ISSN: 0268-1242 figure 15B	3,23

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[X] Further documents are listed in the continuation of box C. [X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
2 October 2001	10/10/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Nesso, S

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INTERNATIONAL SEARCH REPORT

Int. al Application No
PCT/US 01/15892

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5 241 197 A (MURAKAMI EIICHI ET AL) 31 August 1993 (1993-08-31) column 3, line 35 -column 4, line 59; figures 2A,4	15,16
Y	KONIG U ET AL: "Design rules for n-type SiGe hetero FETs" SOLID STATE ELECTRONICS, ELSEVIER SCIENCE PUBLISHERS, BARKING, GB, vol. 41, no. 10, 1 October 1997 (1997-10-01), pages 1541-1547, XP004097077 ISSN: 0038-1101 page 1546, column 1, line 2 - line 5	30-43
A	SCHAEFFLER F: "REVIEW ARTICLE. HIGH-MOBILITY SI AND GE STRUCTURES" SEMICONDUCTOR SCIENCE AND TECHNOLOGY, INSTITUTE OF PHYSICS. LONDON, GB, vol. 12, no. 12, 1 December 1997 (1997-12-01), pages 1515-1549, XP000724834 ISSN: 0268-1242 figure 24	1-48
A	WELSER J ET AL: "ELECTRON MOBILITY ENHANCEMENT IN STRAINED-SI N-TYPE METAL-OXIDE-SEMICONDUCTOR FIELD-EFFECT TRANSISTORS" IEEE ELECTRON DEVICE LETTERS, IEEE INC. NEW YORK, US, vol. 15, no. 3, 1 March 1994 (1994-03-01), pages 100-102, XP000439165 ISSN: 0741-3106 page 100, column 2, line 16 -page 101, column 1, line 24; figure 1B	1-48
A	MIZUNO T ET AL: "HIGH PERFORMANCE STRAINED-SI P-MOSFETS ON SIGE-ON-INSULATOR SUBSTRATES FABRICATED BY SIMOX TECHNOLOGY" INTERNATIONAL ELECTRON DEVICES MEETING 1999. IEDM. TECHNICAL DIGEST. WASHINGTON, DC, DEC. 5 - 8, 1999, NEW YORK, NY: IEEE, US, 1 August 2000 (2000-08-01), pages 934-936, XP000933322 ISBN: 0-7803-5411-7 the whole document	1-48

Form PCT/ISA/210 (continuation of second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Int[illegible]al Application No
PCT/US 01/15892

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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		JP 10308503 A	17-11-1998
		TW 388969 B	01-05-2000
		US 6059895 A	09-05-2000
US 5241197 A	31-08-1993	JP 2196436 A	03-08-1990
		JP 3016230 A	24-01-1991
		EP 0380077 A2	01-08-1990

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(21) International Application Number: PCT/US01/24614

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(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/223,595 7 August 2000 (07.08.2000) US

(71) Applicant: AMBERWAVE SYSTEMS CORPORATION [US/US]; 13 Garabedian Drive, Salem, NH 03079 (US).

(72) Inventors: FITZGERALD, Eugene, A.; 7 Camelot Road, Windham, NH 03087 (US). HAMMOND, Richard; 16 St Paul Street, Apt. 1, Cambridge, MA 02139 (US). CURRIE, Matthew; 36 Symphony Road, Apt. 1A, Boston, MA 02115 (US).

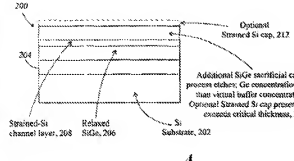
(74) Agent: CONNORS, Matthew, E.; Samuels, Gauthier & Stevens, LLP, 225 Franklin Street, Suite 3300, Boston, MA 02110 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

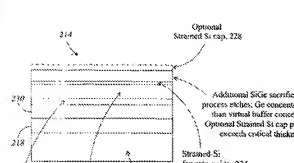
(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European

[Continued on next page]

(54) Title: GATE TECHNOLOGY FOR STRAINED SURFACE CHANNEL AND STRAINED BURIED CHANNEL MOSFET DEVICES



A



B

(57) Abstract: A semiconductor structure including a relaxed $Si_{1-y}Ge_y$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a sacrificial $Si_{1-y}Ge_y$ layer. The sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer. The dielectric layer includes a gate dielectric of a MOSFET. In alternative embodiments, the structure includes a $Si_{1-x}Ge_x$ spacer layer and a Si layer. In another embodiment of the invention there is provided a method of fabricating a semiconductor device including providing a semiconductor heterostructure, the heterostructure having a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on the relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer; removing the $Si_{1-y}Ge_y$ layer; and providing a dielectric layer.

WO 02/13262 A2

patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

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GATE TECHNOLOGY FOR STRAINED SURFACE CHANNEL AND STRAINED BURIED CHANNEL MOSFET DEVICES

PRIORITY INFORMATION

This application claims priority from provisional application Ser. No. 60/223,595 filed August 7, 2000.

BACKGROUND OF THE INVENTION

The invention relates to gate technology for strained surface channel and strained buried channel MOSFET devices.

The advent of high quality relaxed SiGe layers on Si has resulted in the demonstration of field effect transistors (FETs) with carrier channels enhanced via strain. The strain can be incorporated in the channel due to the lattice mismatch between the channel and the relaxed SiGe created by a change in the Ge concentration between the channel layer and the relaxed SiGe layer. For example, a Ge concentration of 20% Ge in the relaxed buffer is high enough such that a thin strained Si layer can exhibit electron mobilities as high as1000-2900 cm^2/V-sec. Also, if the Ge concentration in the channel is greater than the concentration in the buffer, hole channel mobilities can be enhanced. For example, a relaxed buffer concentration of 60-70% Ge can compressively strain a Ge channel layer, creating potentially extremely high hole mobilities.

Although the exact physics of carrier scattering are not known inside short-channel FETs, one thing is clear: these enhanced mobilities translate into increased device performance, even at very short gate lengths. In addition to higher speed and a different power-delay product, the use of strained channels allows for the incorporation of new FET structures into Si-based circuits. Thus, it is anticipated that the high performance, new flexibility in device design, and economics of using a Si-based platform will lead to a plethora of new circuits and products.

With regards to these new circuits and products, the devices based on metal-insulator-semiconductor (MIS) or metal-oxide-semiconductor (MOS) gate technology are the most intriguing, since these devices can follow very closely the processes already used in Si VLSI manufacturing. Two main types of devices are of particular interest: the surface channel device and the buried channel device, examples of which are shown in

FIGs. 1A and 1B.

FIG. 1A is a cross section of a block diagram of a strained Si surface channel device 100, in which a thin strained Si layer 102 is grown atop a relaxed SiGe virtual substrate. The SiGe virtual substrate can be relaxed SiGe 104 on a SiGe graded buffer 105 (as shown in Figure 1a), relaxed SiGe directly on a Si substrate 106, or relaxed SiGe on an insulator such as SiO_2. The device also includes a SiO_2 layer 108 and gate material 110.

FIG. 1B is a cross section of a block diagram of a strained Si buried channel device 112, in which a SiGe layer 116 and a second strained Si layer 120 (used for gate oxidation) cap the strained Si channel layer 114. The structure also includes a graded SiGe buffer layer125 and a second relaxed SiGe layer 126. In both device configurations, a gate oxide 122 is grown or deposited and the gate material 124 is deposited to form the (MOS) structure. Although only devices with strained Si channels are shown in FIGs. 1A and 1B, the invention is applicable to any heterostructure device fabricated on a relaxed SiGe platform. For example, the heterostructure strained channel could be Ge or SiGe of a different Ge content from that of the underlying SiGe virtual substrate. However, the following description will focus on the applicability of the invention to the strained Si device variants illustrated in FIGs. 1A and 1B.

In order to form the MOS gate of the heterostructure device, the SiGe would ideally be oxidized directly in the buried channel device, and the strained Si would be oxidized directly in the surface channel device. Unfortunately, there are problems due to the nature of the Si/SiGe heterostructures in both cases that render the direct oxidation process unsatisfactory.

First consider the surface channel device. Since Si is being oxidized, the interface state density at the resulting SiO_2/Si interface is low, and an electrically high quality interface results. However, all oxidation and cleaning processes during the device and circuit fabrication consume the Si material. In conventional Si processing, there is generally little worry about Si consumption since so little material is consumed compared to any limiting vertical dimension early in the fabrication process. However, in the case of the strained surface channel FET described here, the top strained Si layer is typically less than 300Å thick, and thus too much Si consumption during cleaning and oxidation steps will eliminate the high mobility channel.

One obvious solution is to simply deposit extra Si at the surface, planning for the removal of the Si that occurs during processing. However, the channel strain, which gives the channel its higher carrier mobility, limits the Si layer thickness. At a great enough thickness, the Si layer will begin to relax, introducing misfit dislocations at the Si/SiGe interface. This process of dislocation introduction has two deleterious effects on device performance. First, the strain in the Si is partially or completely relieved, potentially decreasing the carrier mobility enhancements. Second, dislocations can scatter carriers, decreasing carrier mobility. Dislocations can also affect device yield, reliability, and performance.

The buried channel case appears to be a better situation at first, since the Si layer thickness is buried. However, in this case, direct oxidation of SiGe creates a very high interface state density at the oxide/SiGe interface, leading to poor device performance. A known solution in the field is to create a thin Si layer at the surface of the buried channel structure. In this structure, the surface layer is carefully oxidized to nearly consume the entire top Si layer. However, a thin layer of un-oxidized Si is left so that the interface to the oxide is the superior SiO_2/Si interface rather than the problematic oxide/SiGe interface. Although this sacrificial surface Si layer solves the interface electronic property issue, the structure now has the same limits as the structure described above, i.e., the sacrificial Si layer will be slowly etched away during Si processing, possibly leading to exposure of the SiGe and degradation of the electrical properties of the interface as described.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the invention there is provided a semiconductor structure including a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a sacrificial $Si_{1-y}Ge_y$ layer. In one aspect, the sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer. The dielectric layer includes a gate dielectric of a MISFET. In alternative embodiments the structure includes a $Si_{1-y}Ge_y$ spacer layer and a Si layer.

In accordance with another embodiment of the invention there is provided a method of fabricating a semiconductor device including providing a semiconductor heterostructure, the heterostructure having a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a

strained channel layer on the relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer; removing the $Si_{1-y}Ge_y$ layer; and providing a dielectric layer. The dielectric layer includes a gate dielectric of a MISFET. In alternative embodiments, the heterostructure includes a SiGe spacer layer and a Si layer.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1A and 1B are cross sections of block diagrams of strained Si surface and buried channel devices, respectively;

FIGs. 2A and 2B are cross sections of block diagrams of starting heterostructures for surface channel and buried channel strained MOS, respectively, in accordance with the invention;

FIGs. 3A–3D are block diagrams showing the process sequence for a strained surface channel MOS device;

FIGs. 4A–4D are block diagrams showing the process sequence utilizing the gate structure for a buried channel device;

FIG. 5 is a graph of oxidation rates, under a wet oxidation ambient at 700°C, of SiGe alloys, with Ge contents of 0.28 and 0.36, compared to the oxidation rate of bulk silicon;

FIG. 6 is a graph showing the oxide thickness of both a $Si_{0.7}Ge_{0.3}$ alloy and a $Si/Si_{0.7}Ge_{0.3}$ heterostructure;

FIG. 7 is a cross-sectional transmission electron micrograph (XTEM) of the $Si/Si_{0.7}Ge_{0.3}$ heterostructure;

FIG. 8 is a XTEM image of the identical $Si/Si_{0.7}Ge_{0.3}$ heterostructure after wet oxidation followed by oxide removal via a wet etch;

FIG. 9 is a structure for a buried channel MOSFET using relaxed SiGe and strained Si in accordance with the invention; and

FIG. 10 is a graph showing a plot of the middle SiGe layer thickness (h2) and the resulting misfit dislocation spacing.

DETAILED DESCRIPTION OF THE INVENTION

To eliminate the issue of losing valuable surface Si, an innovative step that has

not been previously considered can be employed. In fact, any interest in this area is dominated by discussions of how to change the Si device and circuit process to conserve Si consumption. Although these are certainly possibilities, such constraints severely limit process flexibility, alter the process further from the conventional Si process, and most likely will increase the cost of the fabrication process.

A solution for the buried channel and surface channel structures is to actually deposit another SiGe layer after the desired device structure (which, in the buried channel heterostructure, includes the sacrificial Si layer for oxidation). The structures are shown in FIGs. 2A and 2B.

FIG. 2A is a cross section of a block diagram of a starting heterostructure 200 for surface channel strained MOS in accordance with the invention. The structure 200 includes a Si substrate 202, a SiGe graded buffer 204, a relaxed SiGe layer 206, and a strained-Si channel layer 208. FIG. 2B is a cross section of a block diagram of a starting heterostructure 214 for buried channel strained Si MOS. The structure 214 includes a Si substrate 216, a SiGe graded buffer 218, relaxed SiGe layers 220 and 230, a first strained-Si channel layer 222 and a second strained-Si layer 224 for the gate oxide.

These structures are identical to those depicted in FIGs. 1A and 1B before the gate stack formation, except for the addition of a SiGe capping layer 210, 226 and an optional Si capping layer 212, 228. Since the SiGe layer 210, 226 is closely lattice-matched to the relaxed SiGe layer below the device layers, there is essentially no limit on the thickness of the SiGe layer. This SiGe layer thickness can be tuned to the thickness of material removed before gate oxidation, so that the strained Si layer is exposed just before oxidation. Alternatively, the SiGe can be thicker than the removal thickness and then can be selectively removed. In fact, as described below, SiGe can be selectively removed with respect to Si using a variety of conventional Si-based processes. Therefore, cleaning and oxidation steps can be performed during the Si device and circuit fabrication process with little worry of consuming the precious strained Si and/or the sacrificial strained Si. One only needs to create a SiGe thick enough such that it is not totally consumed before the critical gate oxidation step.

An additional option can be to place yet another Si layer 212, 228 on top of the additional SiGe layer 210, 226. In some processing facilities, the idea of SiGe on the surface, instead of Si, is a factor for concern. In this case, another Si layer can be

deposited on top of the additional SiGe layer described above. By choosing the Ge concentration in the additional SiGe layer to be greater than that of the virtual buffer, a compressive layer can be created; thus, if this additional optional Si layer is greater than the critical thickness, there is no possibility of dislocations moving into the device layers. This phenomenon occurs since the Si layers are tensile, and therefore dislocations introduced into the top optional Si layer have a Burgers vector that will not allow them to glide favorably in the compressive layer below. The dislocations in the top optional Si layer (if the Si layer critical thickness is exceeded) will not penetrate into the layers beneath it, and therefore as much Si can be deposited as desired. In fact, this optional Si capping layer need not be strained at all in this case and can serve as a protective sacrificial layer even if it is fully relaxed.

FIGs. 3A-3D are block diagrams showing the process sequence for a strained surface channel MOS device utilizing the gate strucure described above (the process is shown for a structure without an optional strained surface layer). FIG. 3A shows the initial Si/SiGe heterostructure 200 shown in FIG. 2A. FIG. 3B shows the structure after the completion of the initial steps of a Si VLSI process, which could include wet chemical cleans and oxidation steps. Thus, in FIG. 3B, the protective SiGe capping layer 210 has been reduced in thickness, as a portion of the layer has been consumed during processing. Next, the remainder of the protective SiGe capping layer 210 is selectively removed, leaving the underlying Si layer 208 intact and exposed. A sacrificial oxidation step and oxide strip can also be performed at this point to improve the quality of the exposed Si surface.

The resulting structure is shown in FIG. 3C. FIG. 3D shows the final device structure after gate oxidation to form a gate oxide 300, a structure in which the minimum possible amount of Si was consumed prior to the gate oxidation step. Alternatively, at this point an alternate gate dielectric could be deposited on the exposed Si surface. A pristine Si surface is just as important for a high quality interface with many deposited gate dielectrics as it is for a thermally grown SiO_2 gate dielectric.

FIGs. 4A-4D are block diagrams showing the process sequence utilizing the gate structure for a buried channel device (the process is shown for a structure without an optional strained surface layer) using the initial Si/SiGe heterostructure 214 shown in FIG. 2B. The process steps are identical to those of FIGs. 3A-3D, but in the final

heterostructure, the Si channel layer 222 is separated from the gate dielectric 400 by a SiGe spacer layer 220, thus forming a buried channel. Using selective processes to etch down to the buried Si channel or the top Si layer can use the starting heterostructure 214 in FIG. 4A to form a surface channel device. Such a process can result in enhancement mode and depletion mode devices that can in turn be used to create E/D logic circuits as well as a plethora of analog circuits.

In both sequences, an exemplary sequence of steps is: 1. Pre-gate-oxidation cleaning steps and oxidation; 2. Selective etch or oxidation to remove residual protective SiGe layer; 3. Sacrificial oxide formation on Si; 4. Sacrificial oxide strip; 5. Gate oxidation.

It will be appreciated that steps 3 and 4 can be optional, depending on whether there may be a small amount of Ge left on the surface after the selective removal of the SiGe protection layer. When the original heterostructure is grown, the SiGe/Si interface will not be infinitely abrupt, and therefore it is possible to have a small amount of Ge in the optimally pure Si layer. A sacrificial oxide step can be employed to remove an additional small amount of the Si layer to ensure that pure Si is oxidized in the gate oxidation step, ensuring high quality gate oxide.

The second step, the selective removal of the residual SiGe protective material, can be accomplished in a variety of ways. One convenient process is a wet oxidation step, preferably at 750°C or below. Under wet oxidation at these temperatures, SiGe is oxidized at rates that can be 100 times greater than rates oxidizing Si under the same conditions. Thus, in order to expose the Si for gate oxidation, one can simply do a wet oxidation of the SiGe layer and selectively stop at the Si layer. The oxidized SiGe can be stripped to expose the Si. It is important to note here that the low temperature is not only important for the selectivity in the oxidation process, but also the low temperature is important to minimize or prevent the snow-plowing of Ge in front of the oxidation front, a known problem in the direct oxidation of SiGe.

FIG. 5 is a graph of oxidation rates, under a wet oxidation ambient at 700°C, of SiGe alloys, with Ge contents of 0.28 and 0.36, compared to the oxidation rate of bulk silicon. It is evident from the graph that, under such conditions, the oxidation rate of SiGe increases as the Ge content of the film increases.

FIG. 6 is a similar graph, showing the oxide thickness of both a $Si_{0.7}Ge_{0.3}$ alloy and a Si/ $Si_{0.7}Ge_{0.3}$ heterostructure. Again, the oxidation conditions were 700°C in a

wet ambient; however, FIG. 6 depicts very short oxidation durations compared to FIG. 5. The Si/ $Si_{0.7}Ge_{0.3}$ heterostructure consists of a 50Å strained Si buried layer, followed by a 30Å $Si_{0.7}Ge_{0.3}$, a 20Å strained Si layer and finally a 50Å $Si_{0.7}Ge_{0.3}$ capping layer.

A cross-sectional transmission electron micrograph (XTEM) of the Si/$Si_{0.7}Ge_{0.3}$ heterostructure is shown in FIG. 7. It should be noted from FIG. 6 that the presence of strained Si layers in the heterostructure results in a dramatic retardation in the oxidation rate when compared to the oxidation rate of the uniform $Si_{0.7}Ge_{0.3}$. This retardation of the oxidation rate forms the basis of the selective removal of SiGe alloys over strained Si epitaxial layers.

FIG. 8 is a XTEM image of the identical Si/$Si_{0.7}Ge_{0.3}$ heterostructure after wet oxidation at 700°C for 2 minutes followed by oxide removal via a wet etch. It is apparent that the thin strained Si layer is unaffected by the selective oxidation and remains fully intact. Based on the data shown in FIG. 5, an oxidation duration of 2 minutes far exceeds that required to fully oxidize the 50Å $Si_{0.7}Ge_{0.3}$ capping layer of the heterostructure. The very thin dark band, which is apparent on the surface of the strained Si layer, is a snow-plowed high Ge content layer that occurs during oxidation. Such a layer may be removed using a simple chemical clean or a sacrificial oxidation step, either or both of which typically occur prior to the formation of the gate oxide.

Alternatively, the protective SiGe capping layer can be removed via selective dry or wet chemical etching techniques. For example, at high pressures (> 200mT) and low powers, CF_4 dry etch chemistries will etch relaxed SiGe films with high selectivity to Si. Mixtures of hydrofluoric acid (HF), hydrogen peroxide (H_2O_2), and acetic acid (CH_3COOH) will also selectively etch relaxed SiGe layers over Si at selectivities of 300:1 or more. Other potential selective wet chemical mixtures include HF, water (H_2O), and either H_2O_2 or nitric acid (HNO_3).

Additionally, the stability of the entire structure can be improved by increasing the Ge concentration in the intermediate SiGe layer, and also the top SiGe layer if desired. Below, energetic calculations are used to reveal a guide to creating semiconductor layer structures that increase stability with respect to misfit dislocation introduction.

The critical thickness for a buried channel MOSFET using relaxed SiGe and strained Si has been determined using the energy-balance formulation. The structure

considered is the one shown in FIG. 9. The structure 900 includes a 30% SiGe virtual substrate 902 topped by a 80Å strained Si layer 904, a SiGe layer with Ge concentration x2 and thickness h2 906, and an additional 30Å of strained Si 908. Additional stability would result from the addition of an additional SiGe cap layer as described previously. To simplify, the example of FIG. 9 considers only the increased stability created by increasing the Ge concentration (x2) or thickness (h2) of the SiGe intermediate layer. Additionally, since the SiGe cap layer is removed during processing, the stability of the heterostructure with the SiGe cap removed is or primary importance.

In device processing, one must consider the critical thickness of the entire structure with respect to the relaxed virtual substrate. Individual layers that exceed the individual critical thicknesses are not explicitly ruled out, so one practicing the art would have to verify that none of the layers that are introduced into the desired structure exceed the individual layer critical thicknesses. In other words, in the following calculation it is assumed that each layer in the structure is below its critical thickness with respect to the relaxed buffer.

One key to the formulation is to realize that this calculation should be done with respect to the plastic deformation of the layer composite, δ. Then, the dislocation array energy is the same expression regardless of the layer structure. The elastic energy in the individual layers is changed because of δ. In tensile layers, the strain is lowered by δ. In compressive layers, the energy is raised by δ.

Thus, the energy for a dislocation array (per unit area) inserted at the base of the composite is:

$$E_d = 2\delta D(1-\nu\cos\alpha)[\ln(h_T/b)+1]$$

where h_T is the total thickness of the composite ($h_1+h_2+h_3$), α is the angle between the dislocation line and the Burgers vector b, ν is the Poisson ratio, and D is the average shear modulus for a dislocation lying at the interface between the virtual substrate and the composite structure.

The total elastic energy (per unit area) in all the layers is:

$$E_e = \sum_{i=1}^{3} Y\varepsilon_i^2 h_i$$

where Y is the Young's modulus. Thus, the total energy of the system is:

$E_T = E_\delta + E_e$.

The energy can now be minimized with respect to δ (if the energy is lowest with no dislocations, then δ will have a less than or equal to zero value). The value of plastic deformation then is (for the 3 layer example):

$$\delta = \frac{f_1 h_1}{h_T} - \frac{f_2 h_2}{h_T} + \frac{f_3 h_3}{h_T} - \frac{D(1-\upsilon\cos^2\alpha)\left[\ln\left(\frac{h_T}{b}\right)+1\right]}{Y h_T}$$

The examination of this solution reveals that a general formulation for any structure would be (for any structure of n layers):

$$\delta = \sum_i^n \frac{f_i h_i}{h_T} - \frac{D(1-\upsilon\cos^2\alpha)\left[\ln\left(\frac{h_T}{b}\right)+1\right]}{Y h_T}$$

where f has been assigned a negative value for compressive layers and positive value for tensile layers, and hr is the total thickness of the structure:

$$h_T = \sum_i^n h_i .$$

The amount of plastic deformation and resulting misfit dislocation spacing S was calculated for the structure depicted in FIG. 9 as follows:

Lower strained Si layer thickness h1 = 80Å

Upper strained Si layer thickness h3 = 30Å

Middle SiGe layer thickness h2 variable

Middle SiGe layer Ge concentration x2 variable

Virtual substrate Ge concentration: 30%

FIG. 10 is a graph showing a plot of the middle SiGe layer thickness (h2) and the resulting misfit dislocation spacing. The sharp upturn on the plots represents the critical thickness h2 of the middle SiGe layer when the entire composite structure destabilizes and introduces dislocations at the channel/virtual buffer interface. The different curves are for the different compositions in the second layer h2. Very small increases in Ge result in a large jump in stability of the device layers. This suggests that it is possible to stabilize the layer significantly but not have the band structure altered that much. Adding an extra 5-10% Ge into the h2 layer increases the stability

drastically. For example, FIG. 10 indicates that over 100Å of 30% Ge is required to provide the stability of a 20Å layer of 45% Ge content.

Increasing h2 even when the h2 layer is lattice-matched to the virtual buffer increases the stability of the multilayer structure. In the equations above, the effect can be seen to be much weaker than when a compressive strain in h2 is created. When f2 is zero due to lattice matching to the virtual buffer, the increased stability with increasing h2 comes from the fact that h_1 is increasing and therefore decreasing δ (and increasing S).

It will be appreciated that all the calculations are equilibrium calculations, and as usual, one might suspect that these numbers are somewhat conservative, although also consider that the layers possess many threading dislocations that can bend over at the critical thickness, so there are plenty of sources for misfit dislocation generation.

Sacrificial SiGe capping layers provide an innovative method for the protection of thin strained device layers during processing. Such layers shield these critically important strained channel layers from process steps, such as wet chemical cleans and oxidations, which consume surface material. Before the growth or deposition of the gate dielectric, these protective SiGe layers can be selectively removed by standard processes such as oxidation or wet etching, revealing the intact strained device layer. Also presented is a guideline for engineering strained layer stacks such that relaxation via misfit dislocation is prevented. Compressively strained intermediate layers increase the stability of tensile channel layers, and also serve as a barrier for misfit dislocation introduction into the underlying layers.

Although the present invention has been shown and described with respect to several preferred embodiments thereof, various changes, omissions and additions to the form and detail thereof, may be made therein, without departing from the spirit and scope of the invention.

What is claimed is:

CLAIMS

1. A semiconductor structure comprising:

a relaxed $Si_{1-x}Ge_x$ layer on a substrate;

a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer; and

a sacrificial $Si_{1-y}Ge_y$ layer.

2. The structure of claim 1, wherein said sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer.

3. The structure of claim 2, wherein said dielectric layer comprises a gate dielectric of a MISFET.

4. The structure of claim 3, wherein the gate dielectric comprises an oxide.

5. The structure of claim 3, wherein the gate dielectric is deposited.

6. The structure of claim 3, wherein the MISFET comprises a surface channel device.

7. The structure of claim 3, wherein the MISFET comprises a buried channel device.

8. The structure of claim 1, wherein the strained channel comprises Si.

9. The structure of claim 1, wherein x is approximately equal to y.

10. The structure of claim 9 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

11. The structure of claim 1, wherein $y > x$.

12. The structure of claim 11 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

13. The structure of claim 12, wherein the thickness of the sacrificial Si layer is greater than the critical thickness.

14. The structure of claim 1, wherein the substrate comprises Si.

15. The structure of claim 1, wherein the substrate comprises Si with a layer of SiO_2.

16. The structure of claim 1, wherein the substrate comprises a SiGe graded buffer layer on Si.

17. The structure of claim 1 further comprising a $Si_{1-w}Ge_w$ spacer layer.

18. The structure of claim 17, wherein said sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer.

19. The structure of claim 18, wherein said dielectric layer comprises the gate dielectric of a MISFET.

20. The structure of claim 19, wherein the gate dielectric comprises an oxide.

21. The structure of claim 19, wherein the gate dielectric is deposited.

22. The structure of claim 19, wherein the MISFET comprises a buried channel device.

23. The structure of claim 17, wherein the strained channel comprises Si.

24. The structure of claim 17, wherein w is approximately equal to y.

25. The structure of claim 24 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

26. The structure of claim 17, wherein $y > w$.

27. The structure of claim 26 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

28. The structure of claim 27, wherein the thickness of the sacrificial Si layer is greater than the critical thickness.

29. The structure of claim 17, wherein the substrate comprises Si.

30. The structure of claim 17, wherein the substrate comprises Si with a layer of SiO_2.

31. The structure of claim 17, wherein the substrate comprises a SiGe graded buffer layer on Si.

32. The structure of claim 1 further comprising a $Si_{1-w}Ge_w$ spacer layer and a Si layer.

33. The structure of claim 32, wherein said sacrificial $Si_{1-y}Ge_y$ layer is removed before providing a dielectric layer.

34. The structure of claim 33, wherein said dielectric layer comprises the gate dielectric of a MISFET.

35. The structure of claim 34, wherein the gate dielectric comprises an oxide provided by oxidizing said Si layer.

36. The structure of claim 1, wherein y is made greater than x in order to enhance the stability of said semiconductor structure.

37. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, and a $Si_{1-y}Ge_y$ layer;

removing said $Si_{1-y}Ge_y$ layer; and

providing a dielectric layer.

38. The method of claim 37, wherein said $Si_{1-y}Ge_y$ layer is removed by a selective technique.

39. The method of claim 38, wherein said selective technique is wet oxidation below 750°C.

40. The method of claim 38, wherein said selective technique is a wet or dry chemical etch.

41. The method of claim 37, wherein said dielectric layer comprises a gate dielectric of a MISFET.

42. The method of claim 41, wherein the gate dielectric comprises an oxide.

43. The method of claim 41, wherein the gate dielectric is deposited.

44. The method of claim 41, wherein the MISFET comprises a surface channel device.

45. The method of claim 41, wherein the MISFET comprises a buried channel device.

46. The method of claim 37, wherein the strained channel layer comprises Si.

47. The method of claim 37, wherein x is approximately equal to y.

48. The method of claim 47 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

49. The method of claim 37, wherein $y > x$.

50. The method of claim 49 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

51. The method of claim 50, wherein the thickness of the sacrificial Si layer is greater than the critical thickness.

52. The method of claim 37, wherein the substrate comprises Si.

53. The method of claim 37, wherein the substrate comprises Si with a layer of SiO_2.

54. The method of claim 37, wherein the substrate comprises a SiGe graded buffer layer on Si.

55. The method of claim 37, wherein the semiconductor device comprises a MISFET.

56. The method of claim 37, wherein said $Si_{1-y}Ge_y$ layer is removed to expose said strained channel layer.

57. The method of claim 37, wherein said heterostructure further comprises a $Si_{1-w}Ge_w$ spacer layer.

58. The method of claim 57, wherein said dielectric layer comprises the gate dielectric of a MISFET.

59. The method of claim 58, wherein the gate dielectric comprises an oxide.

60. The method of claim 58, wherein the gate dielectric is deposited.

61. The method of claim 58, wherein the MISFET comprises a buried channel device.

62. The method of claim 57, wherein the strained channel comprises Si.

63. The method of claim 57, wherein y is approximately equal to w.

64. The method of claim 63 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

65. The method of claim 57, wherein $w > y$.

66. The method of claim 65 further comprising a sacrificial Si layer on said sacrificial $Si_{1-y}Ge_y$ layer.

67. The method of claim 66, wherein the thickness of the sacrificial Si layer is greater than the critical thickness.

68. The method of claim 57, wherein the substrate comprises Si.

69. The method of claim 57, wherein the substrate comprises Si with a layer of SiO_2.

70. The method of claim 57, wherein the substrate comprises a SiGe graded buffer layer on Si.

71. The method of claim 57, wherein the semiconductor device comprises a MISFET.

72. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$

layer, a $Si_{1-y}Ge_y$ spacer layer, a Si layer, and a $Si_{1-w}Ge_w$ layer;

removing said $Si_{1-w}Ge_w$ layer to expose said Si layer; and

providing a dielectric layer.

73. A method of fabricating a semiconductor device comprising:

providing a semiconductor heterostructure, said heterostructure comprising a relaxed $Si_{1-x}Ge_x$ layer on a substrate, a strained channel layer on said relaxed $Si_{1-x}Ge_x$ layer, a $Si_{1-y}Ge_y$ spacer layer, a Si layer, and a $Si_{1-w}Ge_w$ layer;

removing said $Si_{1-w}Ge_w$ layer to expose said Si layer; and

oxidizing said Si layer.

74. The method of claim 73, wherein the semiconductor device comprises a MOSFET.

75. The method of claim 73, wherein the semiconductor device comprises a buried channel MOSFET.

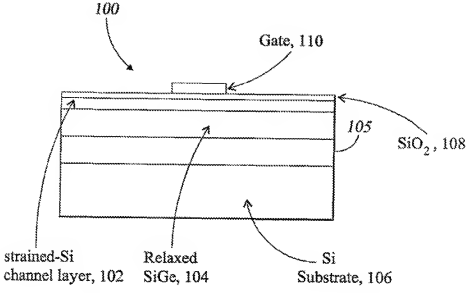
100
Gate, 110
105
SiO_2, 108
strained-Si
channel layer, 102
Relaxed
SiGe, 104
Si
Substrate, 106

FIG. 1A

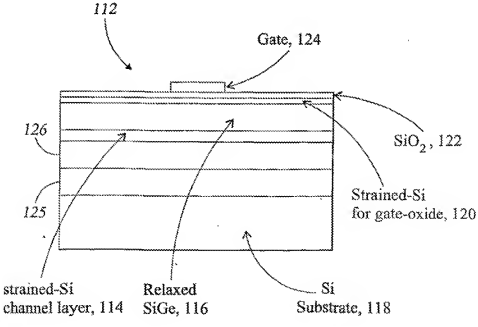
112
Gate, 124
126
125
SiO_2, 122
Strained-Si
for gate-oxide, 120
strained-Si
channel layer, 114
Relaxed
SiGe, 116
Si
Substrate, 118

FIG. 1B

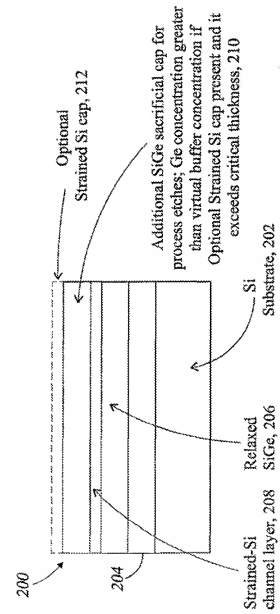
200
204
Strained-Si channel layer, 208
Relaxed SiGe, 206
Si Substrate, 202
Additional SiGe sacrificial cap for process etches; Ge concentration greater than virtual buffer concentration if Optional Strained Si cap present and it exceeds critical thickness, 210
Optional Strained Si cap, 212

FIG. 2A

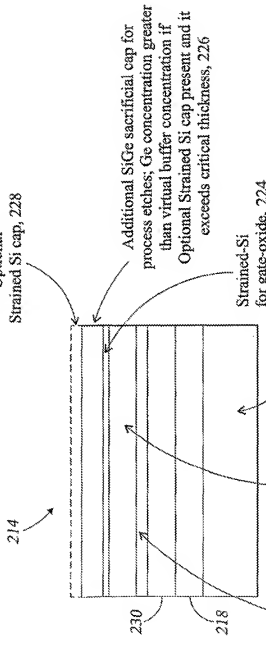
Optional
Strained Si cap, 228
Additional SiGe sacrificial cap for process etches; Ge concentration greater than virtual buffer concentration if Optional Strained Si cap present and it exceeds critical thickness, 226
Strained-Si for gate-oxide, 224
Si Substrate, 216
214
Relaxed SiGe, 220
Strained-Si channel layer, 222
230
218

FIG. 2B

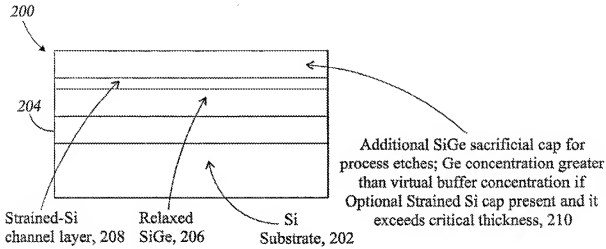
200
204
Additional SiGe sacrificial cap for process etches; Ge concentration greater than virtual buffer concentration if Optional Strained Si cap present and it exceeds critical thickness, 210
Strained-Si channel layer, 208
Relaxed SiGe, 206
Si Substrate, 202

FIG. 3A

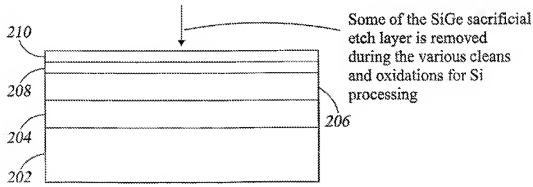
210
208
204
202
206
Some of the SiGe sacrificial etch layer is removed during the various cleans and oxidations for Si processing

FIG. 3B

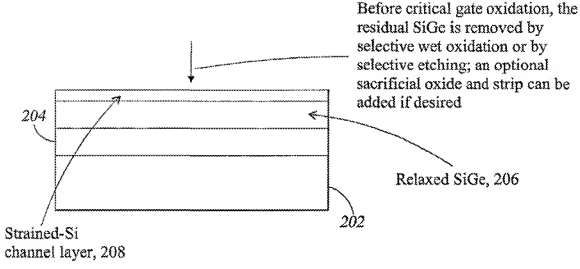
Before critical gate oxidation, the residual SiGe is removed by selective wet oxidation or by selective etching; an optional sacrificial oxide and strip can be added if desired
204
Relaxed SiGe, 206
202
Strained-Si channel layer, 208

FIG. 3C

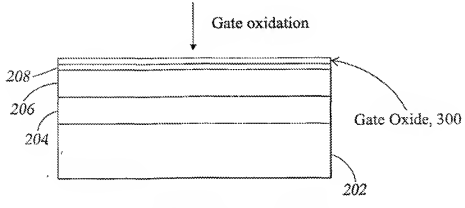
Gate oxidation
208
206
204
Gate Oxide, 300
202

FIG. 3D

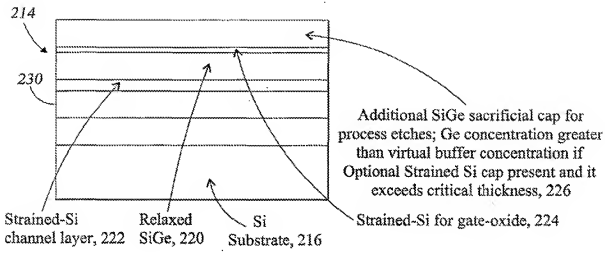
214
230
Additional SiGe sacrificial cap for process etches; Ge concentration greater than virtual buffer concentration if Optional Strained Si cap present and it exceeds critical thickness, 226
Strained-Si channel layer, 222
Relaxed SiGe, 220
Si Substrate, 216
Strained-Si for gate-oxide, 224

FIG. 4A

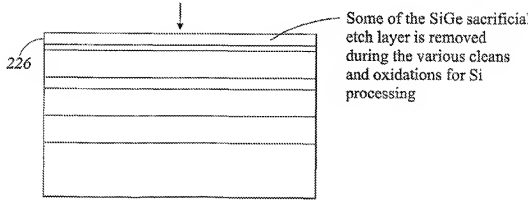
226
Some of the SiGe sacrificial etch layer is removed during the various cleans and oxidations for Si processing

FIG. 4B

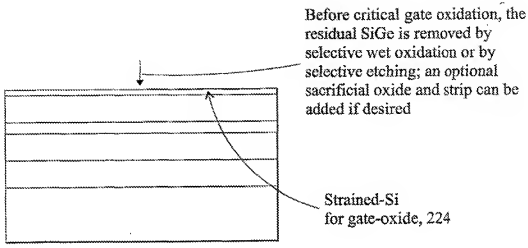
Before critical gate oxidation, the residual SiGe is removed by selective wet oxidation or by selective etching; an optional sacrificial oxide and strip can be added if desired
Strained-Si for gate-oxide, 224

FIG. 4C

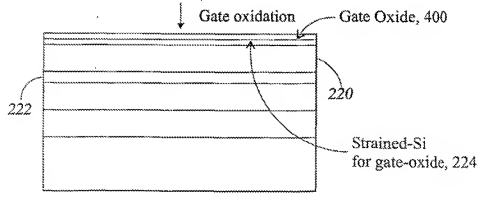
Gate oxidation
Gate Oxide, 400
220
222
Strained-Si for gate-oxide, 224

FIG. 4D

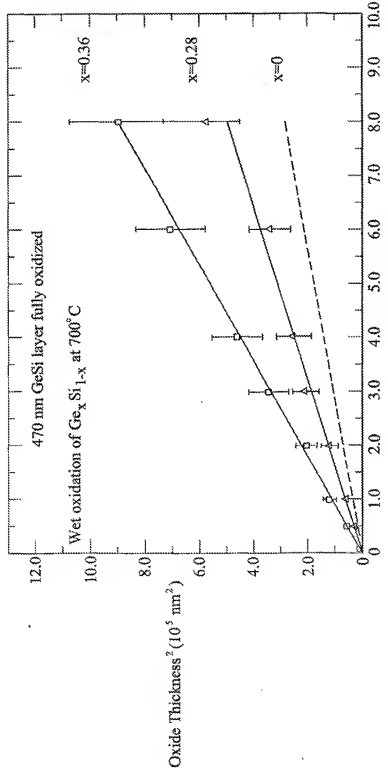
Oxide Thickness^2 (10^5 nm^2)
12.0
10.0
8.0
6.0
4.0
2.0
0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
Oxidation Duration (hr)
470 nm GeSi layer fully oxidized
Wet oxidation of Ge_xSi_{1-x} at 700°C
x=0.36
x=0.28
x=0

FIG. 5

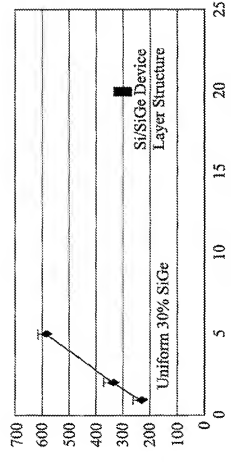
Oxide Thickness (Å)
700
600
500
400
300
200
100
0
0
5
10
15
20
25
700°C Wet Oxidation Time (min)
Si/SiGe Device
Layer Structure
Uniform 30% SiGe

FIG. 6

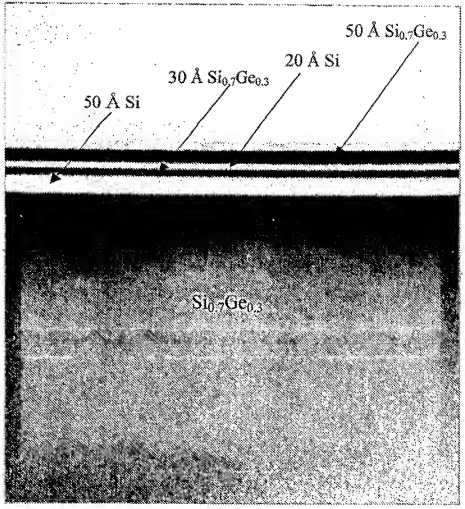

FIG. 7

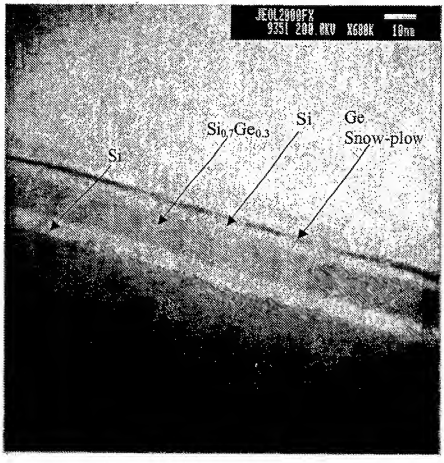
JEOL2000FX
9351 200.0KV X600K 10nm
Si
$Si_{0.7}Ge_{0.3}$
Si
Ge
Snow-plow

FIG. 8

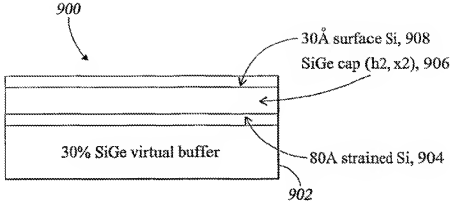
900
30Å surface Si, 908
SiGe cap (h2, x2), 906
30% SiGe virtual buffer
80A strained Si, 904
902

FIG. 9

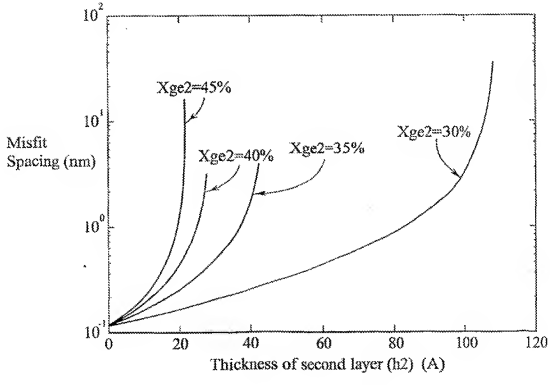
Misfit Spacing (nm)
Xge2=45%
Xge2=40%
Xge2=35%
Xge2=30%
Thickness of second layer (h2) (A)

FIG. 10